Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application:

Listing of Claims:

1. (currently amended) A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:
a mixer core having a doubly balanced mixer including a first differentially coupled transistor pair and a second differentially coupled transistor pair;
an RF input circuit coupled to the mixer core, the RF input circuit comprising:
an ~~input~~ first inductor having a first terminal coupled to receive an RF input signal and a second terminal;
a biasing resistor having a first terminal coupled to the second terminal of the ~~input~~ first inductor and a second terminal coupled to a first bias voltage;
a first input transistor having a ~~control~~ first terminal coupled to the second terminal of the ~~input~~ first inductor, a second terminal, and a third terminal;
a second inductor having a first terminal coupled to the second terminal of the first input transistor and to the first differentially coupled transistor pair, the second inductor also having a second terminal coupled to a ground potential;
a supply resistor having a first terminal coupled to the ~~second~~ third terminal of the first input transistor and a second terminal coupled to a supply potential;
a first capacitor having a first terminal also coupled to the ~~second~~ third terminal of the first input transistor and a second terminal coupled to the second differentially coupled transistor pair; and
a third inductor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the ground potential.

2. (original) The mixer circuit according to Claim 1 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all npn transistors.

3. (original) The mixer circuit according to Claim 1 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all pnp transistors.

4. (original) The mixer circuit according to Claim 1 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MOSFET transistors.

5. (original) The mixer circuit according to Claim 1 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MESFET transistors.

6. (currently amended) A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:
a mixer core having a doubly balanced mixer including a first differentially coupled transistor pair and a second differentially coupled transistor pair, the mixer core coupled to receive a LO drive signal, the LO drive signal having a plurality of harmonics;
a low noise RF input circuit coupled to the mixer core through a folded cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the folded cascode circuit further isolates the low noise RF input circuit from the LO drive signal and the plurality of harmonics.

7. (currently amended) ~~A~~ The mixer circuit as in Claim 6 wherein the folded cascode circuit comprises:
a first cascode transistor having an emitter terminal coupled to a second terminal of a first capacitor and to a first terminal of a ~~third~~ first inductor, a collector terminal coupled to the second differentially coupled transistor pair and a base terminal,
a second cascode transistor having a base terminal coupled to the base terminal of the first cascode transistor, an emitter terminal coupled to a first terminal of a second inductor and to an emitter terminal of a first transistor, and a collector terminal coupled to the first differentially coupled transistor pair,

a second capacitor, having a first terminal coupled to the emitter terminal of the second cascode transistor and a second terminal coupled to ~~a~~ the second terminal of the first capacitor, the base terminal of the first cascode transistor and to the base terminal of the second cascode transistor,

a third capacitor, having a first terminal coupled to the emitter terminal of the first cascode transistor and a second terminal coupled to the second terminal of the second capacitor,

a ~~second biasing~~ first resistor having a first terminal coupled to the first terminal of the second capacitor and a second terminal coupled to a second bias voltage.

8. (currently amended) ~~A~~ The mixer circuit as in Claim 7, wherein the low noise RF input circuit further includes a RF feedback circuit, the RF feedback circuit comprising:

a second transistor having a base terminal coupled to the supply potential, an emitter terminal coupled to ~~the~~ a collector terminal of the first ~~input~~ transistor and a collector terminal coupled to ~~the~~ a first terminal of ~~the~~ a supply resistor and to ~~the~~ a first terminal of the first capacitor,

a feedback resistor, having a first terminal coupled to ~~the~~ a base terminal of the first ~~input~~ transistor and a second terminal,

a ~~second~~ fourth capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

9. (currently amended) ~~A~~ The mixer circuit as in Claim 7, wherein the mixer core further includes a tracking supply circuit, the tracking supply circuit comprising:

a first diode-connected transistor having a cathode terminal coupled to ~~the~~ a ground potential and an anode terminal,

a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal,

a ~~third~~ first resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal,

a first current supply having a first terminal coupled to the second terminal of the ~~third~~ first resistor and a second terminal coupled to the supply potential,

a loop amplifier having a first terminal coupled to the second terminal of the ~~third~~ first resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal,

a ~~fourth~~ second resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal,

a ~~second~~ third transistor having a collector terminal coupled to the second terminal of the ~~fourth~~ second resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal,

a ~~third~~ fourth transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second transistor and a collector terminal,

a ~~fifth~~ third resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third transistor

a second current supply having a first terminal coupled to the emitter terminal of the ~~second~~ third transistor and to the emitter terminal of the ~~third~~ fourth transistor and a second terminal coupled to the ground potential,

a first common collector amplifier having a base terminal coupled to the second terminal of the ~~fifth~~ third resistor and to the collector terminal of the ~~third~~ fourth transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input,

a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential,

a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input,

a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

10. (currently amended) ~~A~~ The mixer circuit as in Claim 7, wherein the low noise RF input circuit further includes a tracking mixer bias current circuit coupled to the second bias input terminal, the tracking mixer bias current circuit comprising:

a ~~third~~ second resistor having a first terminal coupled to the supply potential and a second terminal,

a first diode connected transistor having a anode terminal coupled to the second terminal of the ~~third~~ second resistor and a cathode terminal,

a second transistor having a collector terminal coupled to the cathode terminal of the first diode connected transistor, an emitter terminal coupled to the ground potential and a base terminal,

a loop amplifier having a first terminal coupled to the emitter terminal of the first diode connected transistor and to the collector terminal of the second transistor, a second terminal coupled to the second bias voltage and a third terminal,

a ~~fourth~~ third resistor having a first terminal coupled to the base terminal of the second ~~[npn]~~ transistor and a second terminal coupled to the second terminal of the loop amplifier and to the second bias voltage,

a bandgap voltage supply having a first terminal coupled to the ground potential and a second terminal coupled to the third terminal of the loop amplifier.

11. (currently amended) ~~A~~ The mixer circuit as in Claim 6, wherein the mixer core further includes a tracking supply circuit, the tracking supply circuit comprising:

a first diode-connected transistor having a cathode terminal coupled to ~~the~~ a ground potential and an anode terminal,

a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal,

a ~~third~~ first resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal,

a first current supply having a first terminal coupled to the second terminal of the ~~third~~ first resistor and a second terminal coupled to the supply potential,

a loop amplifier having a first terminal coupled to the second terminal of the ~~third~~ first resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal,

a ~~fourth~~ second resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal,

a second transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal,

a third transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second transistor and a collector terminal,

a ~~fifth~~ third resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third transistor

a second current supply having a first terminal coupled to the emitter terminal of the second transistor and to the emitter terminal of the third transistor and a second terminal coupled to the ground potential,

a first common collector amplifier having a base terminal coupled to the second terminal of the ~~fifth~~ third resistor and to the collector terminal of the third transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input,

a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential,

a second common collector amplifier having a base terminal coupled to the second terminal of the ~~fourth~~ second resistor and to the collector terminal of the second transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input,

a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

12. (currently amended) ~~A~~ The mixer circuit as in Claim 6, wherein the low noise RF input circuit further includes a RF feedback circuit coupled to the RF input circuit, the RF feedback circuit comprising:

a second transistor having a base terminal coupled to ~~the~~ a supply potential, an emitter terminal coupled to the collector terminal of the first ~~input~~ transistor and a collector terminal coupled to ~~the~~ a first terminal of the supply resistor and to ~~the~~ a first terminal of the first capacitor,

a feedback resistor, having a first terminal coupled to ~~the~~ a base terminal of the first ~~input~~ transistor and a second terminal,

a second capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

13. (currently amended) A quadrature mixer circuit for generating a quadrature IF output responsive to an RF input and a quadrature pair of LO drive signals, comprising:

a mixer core having a first doubly balanced mixer including a first differentially coupled transistor pair and a second differentially coupled transistor pair and a second doubly balanced mixer including a third differentially coupled transistor pair and a fourth differentially coupled transistor pair;

an RF input circuit coupled to the mixer core, the RF input circuit comprising:

an input inductor having a first terminal coupled to receive an RF input signal and a second terminal;

a biasing resistor having a first terminal coupled to the second terminal of the input inductor and a second terminal coupled to a first bias voltage;

a first input transistor having a base terminal coupled to the second terminal of the input inductor, an emitter terminal, and a collector terminal;

a second inductor having a first terminal coupled to the emitter of the first input transistor and to the first differentially coupled transistor pair and to the

third differentially coupled transistor pair, the second inductor also having a second terminal coupled to a ground potential;

a supply resistor having a first terminal coupled to the collector of the first input transistor and a second terminal coupled to a supply potential;

a first capacitor having a first terminal also coupled to the collector of the first transistor and a second terminal coupled to the second differentially coupled transistor pair and to the fourth differentially coupled transistor pair; and

a third inductor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the ground potential.

14. (currently amended) A quadrature mixer circuit for generating a quadrature IF output responsive to an RF input and a quadrature pair of LO drive signals, comprising:

a mixer core having a first doubly balanced mixer including a first differentially coupled transistor pair and a second differentially coupled transistor pair and having a second doubly balanced mixer including a third differentially coupled transistor pair and a fourth differentially coupled transistor pair; the mixer core coupled to receive a quadrature LO drive signal, the quadrature LO drive signal having a plurality of harmonics;

a low noise RF input circuit coupled to the mixer core through a folded cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the folded cascode circuit further isolates the low noise RF input circuit from the quadrature LO drive signal and the plurality of harmonics,

a first cascode capacitor, a first terminal of the first cascode capacitor coupled to ~~the~~ an emitter terminal of a first cascode transistor and a second node of the first cascode capacitor coupled to ~~the~~ base terminals of the first cascode transistor and a second cascode transistor,

a second cascode capacitor, a first terminal of the second cascode capacitor coupled to the base terminals of the first cascode transistor and the second cascode transistor and ~~the~~ a second node of the second cascode capacitor coupled to ~~the~~ an emitter terminal of the second cascode transistor.

15. (currently amended) ~~A~~ The quadrature mixer circuit as in Claim 14 wherein the folded cascode circuit comprises:

a first cascode transistor having an emitter terminal coupled to ~~the~~ a second terminal of ~~the~~ a first capacitor and to ~~the~~ a first terminal of ~~the third~~ a first inductor, a collector terminal coupled to the second differentially coupled transistor pair and a base terminal,

a second cascode transistor having a base terminal coupled to the base terminal of the first cascode transistor, an emitter terminal coupled to ~~the~~ a first terminal of ~~the~~ a second inductor and to the emitter terminal of the first transistor and a collector terminal coupled to the first differentially coupled transistor pair,

~~a second capacitor, having a first terminal coupled to the collector terminal of the first cascode transistor and a second terminal coupled to the base terminal of the first cascode transistor and to the base terminal of the second cascode transistor;~~

~~a third capacitor, having a first terminal coupled to the emitter terminal of the second cascode transistor and a second terminal coupled to the second terminal of the second capacitor and to the base terminal of the first cascode transistor and to the base terminal of the first second cascode transistor;~~

a ~~second biasing~~ first resistor having a first terminal coupled to the second terminal of the ~~second~~ first cascode capacitor and the first terminal of the ~~third~~ first cascode capacitor and a second terminal coupled to a ~~second~~ first bias voltage,

a ~~third biasing~~ second resistor having a first terminal coupled to the ~~second~~ first bias voltage and to the second terminal of the ~~second biasing~~ first resistor and having a second terminal,

a third cascode transistor having a collector terminal coupled to the fourth differentially coupled transistor pair, an emitter terminal coupled to the ~~second~~ first terminal of the ~~third~~ first inductor and to the emitter terminal of the first cascode transistor, and a base terminal,

a fourth cascode transistor having a base terminal coupled to the base terminal of the third cascode transistor, a collector terminal coupled the third differentially coupled transistor pair and an emitter terminal coupled to the emitter terminal of the second cascode transistor and to the ~~second~~ first terminal of the second inductor,

a ~~fourth~~ third cascode capacitor having a first terminal coupled to the emitter terminal of the third cascode transistor and a second terminal coupled to the base terminal of the third and fourth cascode transistors,

a ~~fifth~~ fourth cascode capacitor having a first terminal coupled to the second terminal of the ~~fourth~~ third cascode capacitor and to the base terminals of the third and fourth cascode transistors and a second terminal coupled to the emitter terminal of the fourth cascode transistor.

16. (currently amended) ~~A~~ The quadrature mixer circuit as in Claim 15 wherein the low noise RF input circuit further includes a RF feedback circuit, the RF feedback circuit comprising:

a second transistor having a base terminal coupled to ~~the~~ a supply potential, an emitter terminal coupled to the collector terminal of the first ~~input~~ transistor and a collector terminal coupled to ~~the~~ a first terminal of the supply resistor and to ~~the~~ a first terminal of the first capacitor,

a feedback resistor, having a first terminal coupled to ~~the~~ a base terminal of the first input transistor and a second terminal,

a ~~sixth~~ second capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

17. (currently amended) ~~A~~ The quadrature mixer circuit as in Claim 16, wherein the mixer core further includes a first tracking supply circuit portion coupled to ~~the~~ In-Phase LO drive input terminals of the mixer core and a second tracking supply circuit portion coupled to ~~the~~ Quadrature Phase LO drive input terminals of the mixer core.

18. (currently amended) ~~A~~ The quadrature mixer circuit as in Claim 17, wherein the first tracking supply circuit portion comprises:

a. a first diode-connected transistor having a cathode terminal coupled to ~~the~~ a ground potential and an anode terminal;

b. a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal,

c. a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal;

d. a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential;

e. a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal;

f. a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal;

g. a ~~second~~ third transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and an emitter terminal;

h. a ~~third~~ fourth transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the ~~second~~ third transistor and a collector terminal;

i. a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the ~~third~~ fourth transistor;

j. a second current supply having a first terminal coupled to the emitter terminal of the ~~second~~ third transistor and to the emitter terminal of the ~~third~~ fourth transistor and a second terminal coupled to the ground potential;

k. a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the ~~third~~ fourth transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input;

l. a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential;

m. a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the ~~second~~ third transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input; and

n. a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential;

and wherein the second tracking supply circuit portion comprises:

o. a third diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal;

p. a fourth diode-connected transistor having a cathode terminal coupled to the anode terminal of the third diode connected transistor and an anode terminal;

q. a ~~third~~ sixth resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal;

r. a ~~first~~ fifth current supply having a first terminal coupled to the second terminal of the ~~third~~ sixth resistor and a second terminal coupled to the supply potential;

s. a second loop amplifier having a first terminal coupled to the second terminal of the ~~third~~ sixth resistor and to the first terminal of the ~~first~~ fifth current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal;

t. a ~~fourth~~ seventh resistor having a first terminal coupled to the fourth terminal of the second loop amplifier and a second terminal;

u. a ~~second~~ fourth transistor having a collector terminal coupled to the second terminal of the ~~fourth~~ seventh resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal;

v. a ~~third~~ fourth transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the ~~second~~ fourth transistor and a collector terminal;

w. a ~~fifth~~ eighth resistor having a first terminal coupled to the fourth terminal of the second loop amplifier and a second terminal coupled to the collector terminal of the ~~third~~ fourth transistor;

x. a ~~second~~ sixth current supply having a first terminal coupled to the emitter terminal of the ~~second~~ fourth transistor and to the emitter terminal of the ~~third~~ fourth transistor and a second terminal coupled to the ground potential;

y. a ~~first~~ third common collector amplifier having a base terminal coupled to the second terminal of the ~~fifth~~ eighth resistor and to the collector terminal of the ~~third~~

fourth transistor, a collector terminal coupled to the fourth terminal of the second loop amplifier, and an emitter terminal coupled to a first mixer core LO input;

z. a ~~third~~ seventh current supply having a first terminal coupled to the emitter terminal of the ~~first~~ third common collector amplifier and a second terminal coupled to the ground potential;

aa. a ~~second~~ fourth common collector amplifier having a base terminal coupled to the second terminal of the ~~fourth~~ seventh resistor and to the collector terminal of the ~~second~~ fourth transistor, a collector terminal coupled to the fourth terminal of the second loop amplifier and an emitter terminal coupled to a second mixer core LO input;

ab. a ~~fourth~~ eighth current supply having a first terminal coupled to the emitter terminal of the ~~second~~ fourth common collector amplifier and a second terminal coupled to the ground potential.

19. (currently amended) ~~A~~ The quadrature mixer circuit as in Claim 15, wherein the low noise RF input circuit further includes a tracking mixer bias current circuit, the tracking bias current circuit comprising:

a first resistor having a first terminal coupled to the supply potential and a second terminal,

a first diode connected transistor having a anode terminal coupled to the second terminal of the third resistor and a cathode terminal,

a second transistor having a collector terminal coupled to the cathode terminal of the first diode connected transistor, an emitter terminal coupled to the ground potential and a base terminal,

a loop amplifier having a first terminal coupled to the emitter terminal of the first diode connected transistor and to the collector terminal of the second transistor, a second terminal coupled to the ~~second~~ first bias voltage and a third terminal,

a second resistor having a first terminal coupled to the base terminal of the second transistor and a second terminal coupled to the second terminal of the loop amplifier and to the ~~second~~ first bias voltage,

a bandgap voltage supply having a first terminal coupled to the ground potential and a second terminal coupled to the third terminal of the loop amplifier.

20. (canceled)

21. (currently amended) A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:
a mixer core having a doubly balanced mixer including a first differentially coupled transistor pair and a second differentially coupled transistor pair, the mixer core coupled to receive a LO drive signal, the LO drive signal having a plurality of harmonics;
a low noise single ended RF input circuit coupled to the mixer core through a cascode circuit, the low noise single ended RF input circuit coupled to receive an RF input signal, wherein the cascode circuit further isolates the low noise single ended RF input circuit from the LO drive signal and the plurality of harmonics, the low noise single ended RF circuit including means for providing an input impedance and means for splitting a phase of the RF input signal.

22. (currently amended) The mixer circuit according to Claim 6 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first ~~input~~ transistor are all npn transistors.

23. (currently amended) The mixer circuit according to Claim 6 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first ~~input~~ transistor are all pnp transistors.

24. (currently amended) The mixer circuit according to Claim 6 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first ~~input~~ transistor are all MOSFET transistors.

25. (currently amended) The mixer circuit according to Claim 6 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first ~~input~~ transistor are all MESFET transistors.

26. (currently amended) The quadrature mixer circuit according to Claim 13 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all npn transistors.

27. (currently amended) The quadrature mixer circuit according to Claim 13 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all pnp transistors.

28. (currently amended) The quadrature mixer circuit according to Claim 13 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all MOSFET transistors.

29. (currently amended) The quadrature mixer circuit according to Claim 13 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all MESFET transistors.

30. (currently amended) The quadrature mixer circuit according to Claim 14 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first ~~input~~ transistor are all npn transistors.

31. (currently amended) The quadrature mixer circuit according to Claim 14 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first ~~input~~ transistor are all pnp transistors.

32. (currently amended) The quadrature mixer circuit according to Claim 14 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the

third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first ~~input~~ transistor are all MOSFET transistors.

33. (currently amended) The quadrature mixer circuit according to Claim 14 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first ~~input~~ transistor are all MESFET transistors.

34. (canceled)

35. (canceled)

36. (canceled)

37. (canceled)

38. (currently amended) The mixer circuit according to Claim 21 wherein the first differentially coupled transistor pair[,] and the second differentially coupled transistor pair ~~and the first input transistor~~ are all npn transistors.

39. (currently amended) The mixer circuit according to Claim 21 wherein the first differentially coupled transistor pair[,] and the second differentially coupled transistor pair ~~and the first input transistor~~ are all pnp transistors.

40. (currently amended) The mixer circuit according to Claim 21 wherein the first differentially coupled transistor pair[,] and the second differentially coupled transistor pair ~~and the first input transistor~~ are all MOSFET transistors.

41. (currently amended) The mixer circuit according to Claim 21 wherein the first differentially coupled transistor pair[,] and the second differentially coupled transistor pair ~~and the first input transistor~~ are all MESFET transistors.